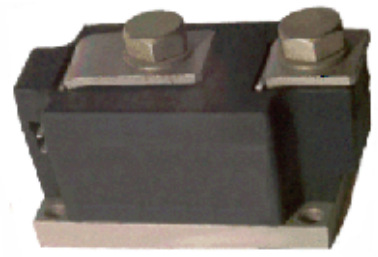
**T R I A C  M O D U L E**

# M1TS-500

- $V_{DRM}$ = **300÷1200 V**
- $I_{TRMS}$ = **500 A** ($T_C$ = 85 °C)
- $I_{TSM}$ = **5.5 kA** ($T_{Vj}$ = 125 °C)



- Heat transfer through AlN ceramic isolated metal baseplate
- Presspack construction
- High reliability at thermal cycles
- double polar drive
- Case width 50 mm

## MAXIMUM RATED VALUES

| Parameter and conditions | Symbol | Values | | | Units |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| Repetitive peak off-state voltage, $T_{Vj}$ = - 60 °C…+ 125 °C | $V_{DRM}$ | 300 | - | 1200 | V |
| Non-repetitive peak off-state voltage, $T_{Vj}$ = - 60 °C…+ 125 °C | $V_{DSM}$ | 400 | - | 1300 | |
| Repetitive peak off-state current, $T_{Vj}$ = 125 °C, $V_D = V_{DRM}$ | $I_{DRM}$ | - | - | 35 | mA |
| Max. average on-state current, f = 50 Hz, $T_C$ = 85 °C | $I_{TRMS}$ | - | - | 500 | A |
| Surge non-repetitive current, $T_{Vj}$ = 125 °C, $t_p$ = 20 ms | $I_{TSM}$ | - | - | 5.5 | kA |
| Critical rate of rise of on-state current, V = 0,67$V_{DRM}$, $I_T$ = 1000 A, $I_{FG}$ = 1 A, $t_r$ = 1 µs, f = 50 Hz, $T_{Vj}$ =125 °C | $(di_T/dt)_{crit}$ | - | - | 25 | A/µs |
| Critical rate of rise of switching voltage, $V_D$ = 0,67$V_{DRM}$, $T_{Vj}$ = 125 °C, $I_T = I_{TRMS}$, $t_P$ = 10 ms | $(dV_D/dt)_{com}$ | 6.3 | - | 100 | V/µs |
| Gate power loss, DC | $P_{GM}$ | - | - | 4 | W |
| Control quadrants | | 1, 3, 4 | | | |
| Operation junction temperature range | $T_{Vj}$ | - 60 | - | + 125 | °C |
| Storage temperature range | $T_{stg}$ | - 60 | - | + 50 | |

# M1TS-500

| | | | | | |
|---|---|---|---|---|---|
| **ELECTRICAL CHARACTERISTICS** | | | | | |
| Maximum peak on-state voltage, $I_T$ = 700 A, $T_{Vj}$ = 25 °C | $V_{TM}$ | - | - | 1.50 | V |
| On-state threshold voltage, $T_{Vj}$ = 125 °C, $I_T$ = 350÷1100 A | $V_{(TO)}$ | - | - | 1.00 | |
| On-state slope resistance, $T_{Vj}$ = 125 °C, $I_T$ = 350÷1100 A | $r_T$ | - | - | 0.67 | mΩ |
| Gate trigger voltage, $V_D$ = 12 V,<br>$T_{Vj}$ = - 60 °C<br>$T_{Vj}$ = 25 °C<br>$T_{Vj}$ = 125 °C | $V_{GT}$ | - | - | 5.5<br>3.0<br>2.5 | V |
| Gate trigger current, $V_D$ = 12 V,<br>$T_{Vj}$ = - 60 °C<br>$T_{Vj}$ = 25 °C<br>$T_{Vj}$ = 125 °C | $I_{GT}$ | - | - | 700<br>300<br>250 | mA |
| Gate non-trigger voltage, $V_D$ = 0,67$V_{DRM}$, $T_{Vj}$ = 125 °C | $V_{GD}$ | 0.25 | - | - | V |
| Insulation test voltage (RMS), f = 50 Hz, t = 1sec/1min | $V_{isol}$ | - | - | 3600/3000 | |
| **THERMAL PARAMETERS** | | | | | |
| Thermal resistance junction to case | $R_{th(j-c)}$ | - | - | 0.064 | °C/W |
| Thermal resistance case to heatsink | $R_{th(c-h)}$ | - | - | 0.020 | |
| **MECHANICAL PARAMETERS** | | | | | |
| Weight | w | - | 0.8 | - | kg |
| Terminal connection torque | $M_t$ | 9 | - | 11 | Nm |
| Heatsink mounting torque | $M_s$ | 4 | - | 6 | Nm |
| Maximum acceleration (at nominal mounting force) | a | - | - | 50 | $m/s^2$ |

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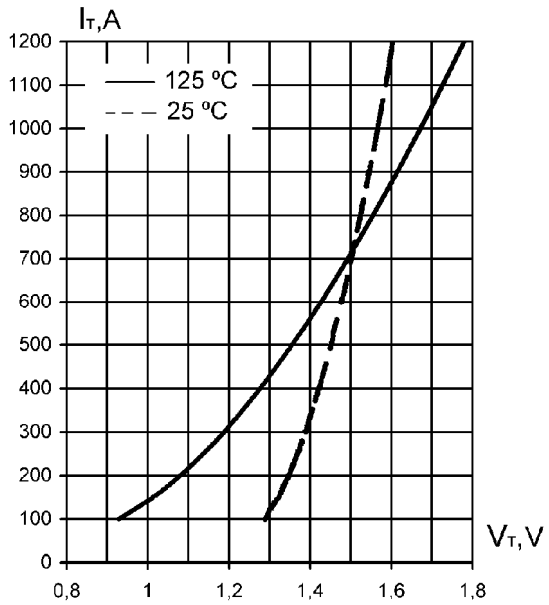


**Fig. 1. Maximum on-state characteristics**
(Limit device, 10 ms, half sine)

**On-state characteristics model**

$V_T = A + B \cdot I_T + C \cdot \ln(I_T + 1) + D \cdot \sqrt{I_T}$

Valid for $I_T$ = 100÷1200 A

| | $T_{Vj}$ = 125 ºC | $T_{Vj}$ = 25 ºC |
|---|---|---|
| A | 0.251 | 1.014 |
| B | 0.0002818 | 0.00008433 |
| C | 0.119 | 0.048 |
| D | 0.01 | 0.0043 |

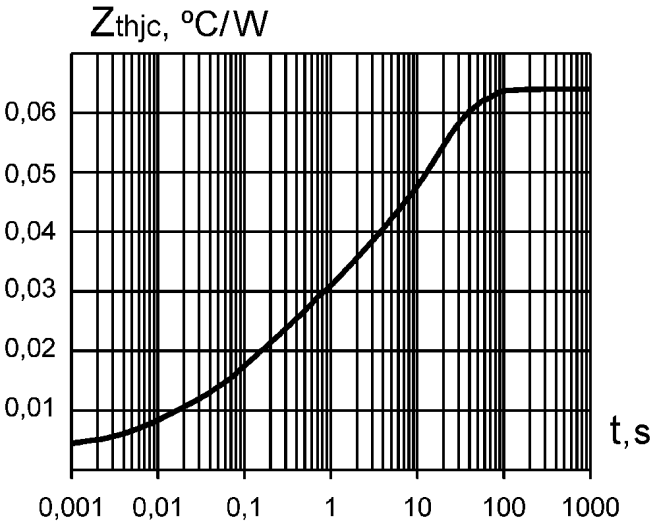


**Fig. 2. Transient thermal impedance junction to case (DC)**

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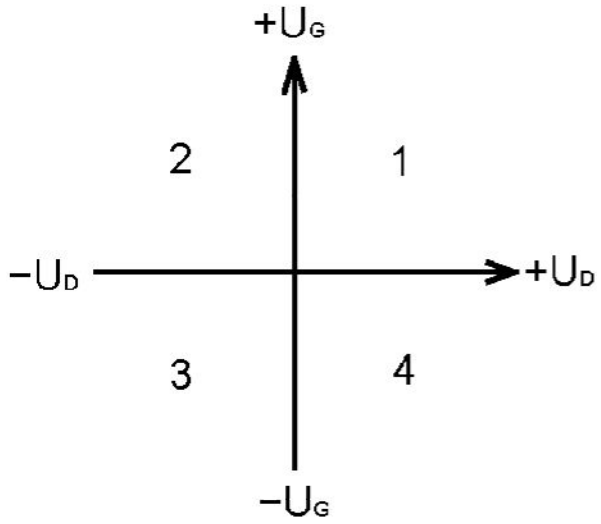


**Fig. 3. Control quadrants**

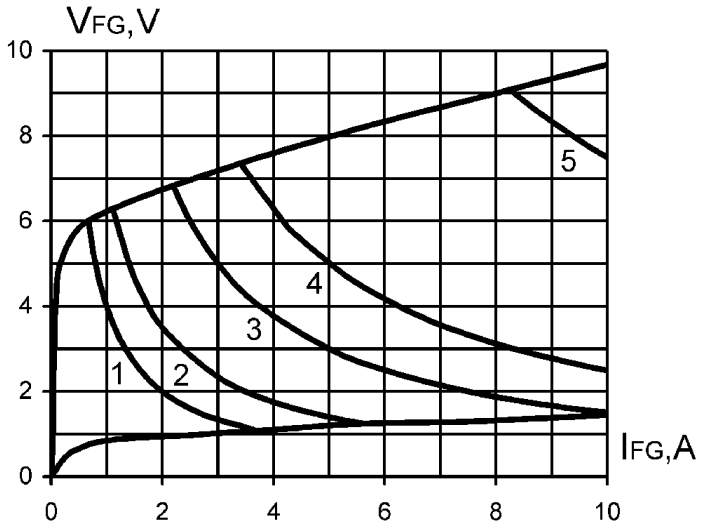


**Fig. 4. Maximum peak gate power losses**

| Position at fig. 4 | Duty cycle, $D = f \cdot t_p$ | Gate pulse length, $t_p$, ms | Maximum gate pulse power $P_{GM}$, W |
|---|---|---|---|
| 1 | 1 | DC | 4 |
| 2 | 2 | 10 | 7 |
| 3 | 20 | 1,0 | 15 |
| 4 | 40 | 0,5 | 25 |
| 5 | 200 | 0,1 | 75 |

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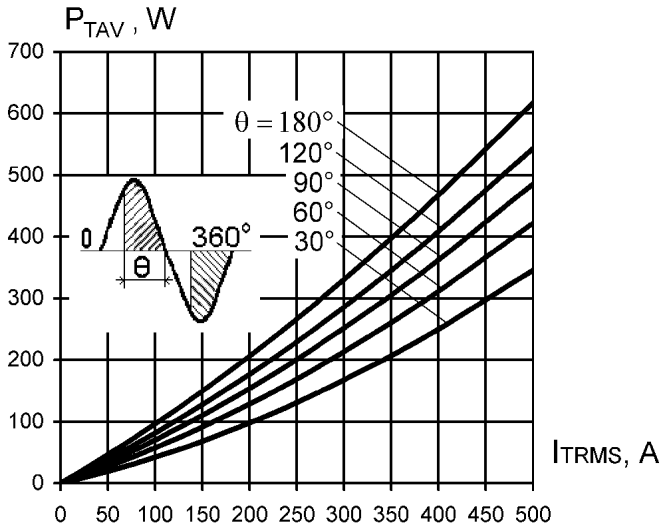


**Fig. 5. Mean power of losses**
(sine)

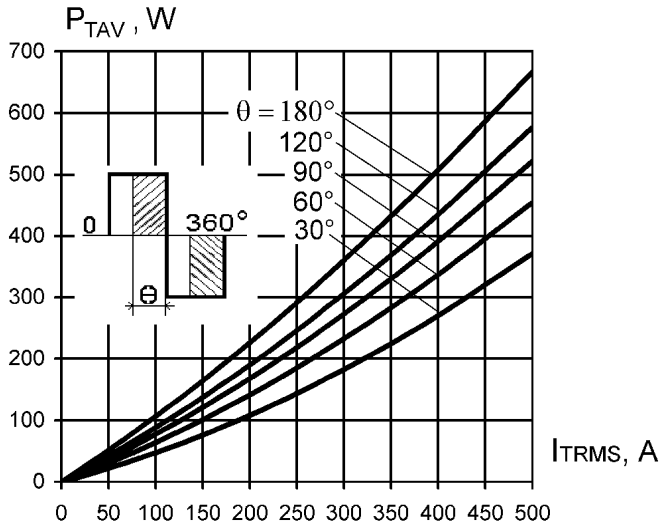


**Fig. 6. Mean power of losses**
(rectangular)

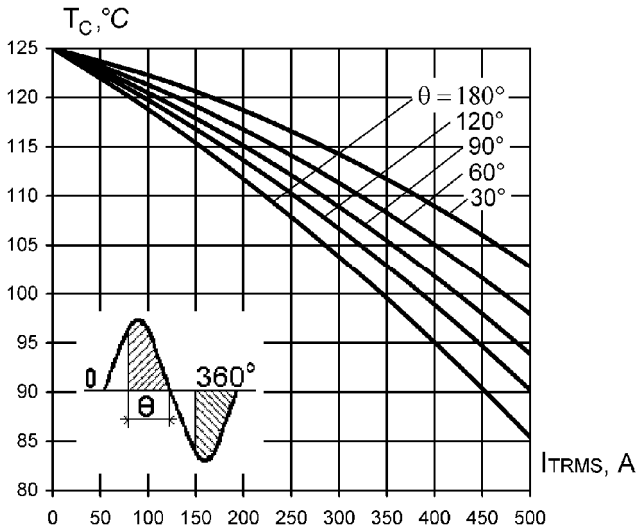


**Fig. 7. Maximum allowable case temperature**
(sine)

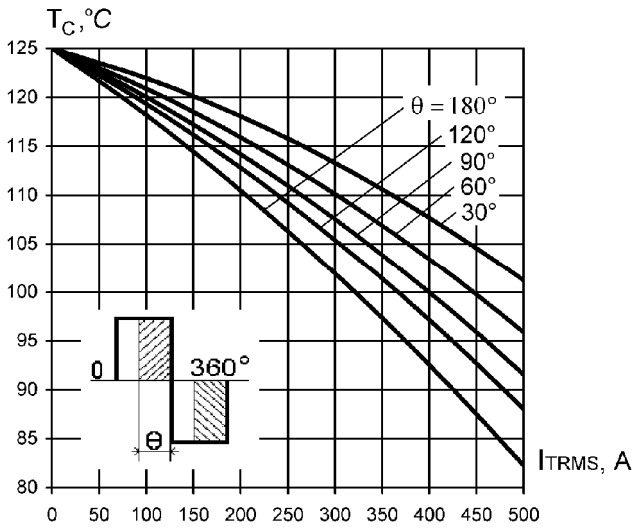


**Fig. 8. Maximum allowable case temperature**
(rectangular)

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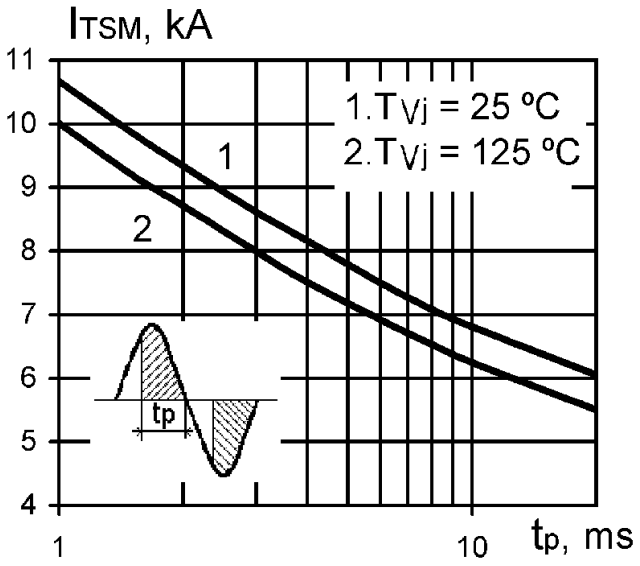


**Fig. 9. Surge on-state current vs. pulse length**

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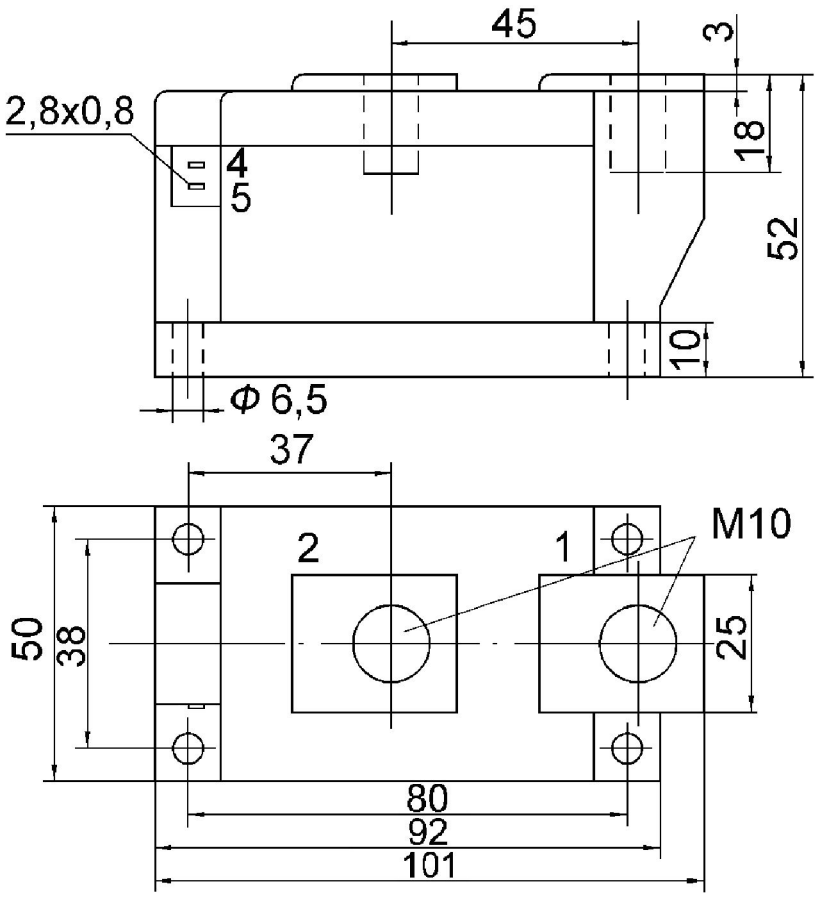
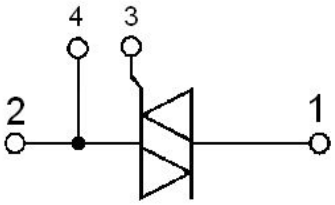



**Fig. 10. Device Outline Drawing**
(dimensions in mm)

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