Development trends of power electronics demand device power increasing, new functional features, high device and system reliability. Using of LTTs allows simple and reliable circuit solutions in variable application fields: power transmission, ultra-high power pulse commutation, high-voltage drives and other. In 70-80 years of last century, after NTD silicon introduction, new possibilities has been opened for high-power high-voltage semiconductor devices.

Investigations of p-n-p-n structure optical triggering were started in Russia 50 years ago. But these investigations were episodic and practically they were the research works. Russian companies offered until recently only small LTTs, optron thyristors and modules with relatively small currents and voltages. Development of LTTs and conventional thyristors with integrated self-protection elements is being in the last 15-20 years the main stream of power semiconductors. Increased power and costs of power electronic systems demand new self-protected (intelligent) device generation. The main aim of integrated self-protection is to prevent irreversible device degradation during error (critical) commutation mode.

This paper presents joint results of All-Russian Electrotechnical Institute and JSC Electrovipryamitel in research, development and production of high-voltage power LTTs.

**LTTs for Phase Control Applications**

LTTs are widely used in modern high effective converters for HVDC transmission and DC links. The cause for that is their advantages by series connection: high robustness and overloading capability, precise temporal control by turning on of thyristor groups, high voltage isolation between control and power circuits, integrated self-protection functions and other.

LTT design is the same as press-pack thyristor one, with optical input instead of electrical gate interface. Optical input is disposed at cathode base center and represents optical window closed by light-sensitive region of semiconductor structure (Figure 1).

Triggering pulse comes into light-sensitive silicon region through optical cable from IR laser diode. Cable length is practically unlimited, because of very low signal attenuation (~1 dB/km). Laser diode converts electrical signal from drive circuit into light pulse with practically identical form and duration. Correct choice of wave length is very important for effective LTT operation. Optimal wave length is stipulated by silicon structure design feature with deep collector p-n junction. Figure 2 illustrates simulated turn-on delay time versus laser diode wave length (pulse power 200 mW).

![Figure 1: LTT design](image1)

![Figure 2: Simulated LTT turn-on delay time versus laser diode wave length](image2)

Simulation shows that optimum wave length for developed LTT triggering lays in range 1000-1050 nm. Wave length over 1100 nm is uneffective because photon energy is insufficient for electron-hole pair generation. Light effectiveness goes down too, when wave...
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length becomes less than 1000 nm, due to low light penetration into silicon and electron-hole pair recombination close to surface.

Creation of gate region with high light sensitivity is big challenge during LTT development. Output optical power of drive system is much lower than input electrical power, despite of advanced light emission sources and optical cables. Thyristor with high optical sensitivity is simultaneously very sensitive to interferences and has low allowable rate of rise of forward off-state voltage $dV_D/dt$. Light sensitive region must be small for ensuring of high $dV_D/dt$, but it limits rate of rise of on-state current $dV_I/dt$.

The developed LTTs are triggered with optical power no more as 20 mW and withstand $dV_D/dt = 5000 \frac{V}{\mu s}$. It was achieved owing to optimal diffusion profile of semiconductor structure, optimal light sensitive and cathode regions layout and amplifying gate structure. Amplifying gate is necessary since photon irradiation of light sensitive region generates very low gate current.

Some specific dangerous modes spring up during power thyristor operation. One of the most critical modes is overvoltage, when applied anode voltage exceeds avalanche breakdown voltage of collector junction that leads to thyristor latch up. It appears in very small region with minimal electric strength and causes current filaments and silicon structure melting.

The aim of integrated overvoltage protection is to form internal gate signal and turn thyristor on before the anode voltage will reach latch up voltage of main structure. Local region with lowered collector junction breakdown voltage is created for this aim in the central region of silicon structure. Avalanche breakdown current arises in this region when anode voltage exceeds breakdown voltage. This current flows to cathode region and turns thyristor on. So this current represents gate triggered current.

Local region with lowered breakdown voltage can be created both inside and outside of light sensitive region. When semiconductor structure has amplifying gate this region can be created inside of any amplifying ring. Local regions with lowered breakdown voltage can be created by means of local n-base resistivity lowering, through shallow donor levels combined with hydrogen atoms.

Operation of integrated self-protection elements was examined in test circuit that forms voltage pulses up to 10 kV. Test arrangement has IR-camera for local breakdown registration in silicon structure. Figure 3 illustrates LTT self-protection [1].

Figure 3a presents voltage and current wave forms – fast forward voltage increase, LTT turn on by $V_D = 6500 \text{ V}$ with following anode current pulse. Figure 3b presents IR image of tested device at self-protection snap instant. Local region with lowered breakdown voltage is visible as hot spot in the center of semiconductor wafer.

Power components for series and parallel connection must be designed so that all devices switch simultaneously and similarly. Reverse recovery charges must be equal. Weak electron irradiation of LTT silicon structures allows to reach minimal technological dispersion of reverse recovery charge values and low commutation overvoltage by optimal on-state voltage ($V_{TH}$).

The main parameters and characteristics of new developed LTTs are presented in table 1.

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Figure 4 shows silicon structure layout of LTT for pulsed power applications. It has high degree interdigitated gate with 4-stage amplifying structure. Interdigitated gate contributes to turn-on time shortening and commutation loss reduction.

Thyristor robustness and reliability during pulse commutation with high $\text{d}I/\text{d}t$ depends on dynamic temperature distribution through silicon structure. High current density at the turn-on beginning leads to overheating of amplifying structure and adjoining cathode region. Temperature distribution in central region was simulated for critical places determination.

Figure 5 shows simulation results. Curve 1 presents temperature distribution for structure with optimal current limiting resistance. Curve 2 concerns LTT structure without integrated current limiting resistor.

As can be seen from simulation results, overheating of gate region at turn-on beginning is main physical factor that limits commutated current $\text{d}I/\text{d}t$. The first amplifying stage is overheated most of all. Temperature in this region can reach the critical value at which current filament arises that leads to thermal destruction. Current filaments arise when thermal generation becomes main conductivity modulation mechanism in n-base local regions. The critical temperature for filamentation beginning is 400-600 °C.

Amplifying structure of special design and integrated current limiting resistors was developed for turn-on loss minimization and high $\text{d}I/\text{d}t$ ensuring. Overheating of first amplifying stage depends on current limiting resistance that can be controlled by means of p-base mesa-etching. It can be seen from figure 5 that R1 region is overheated up to 120 °C when LTT structure is not optimal. Resistance increasing for structure optimization allows 30 °C temperature decreasing. Figure 6 shows experimental dependence of current limiting resistance on technological factors. Figure 7 illustrates experimental dependence of minimal anode voltage on integrated resistance value.

Developed LTT was tested for estimation of maximal pulse commutation capability. Fig. 8 shows anode current and triggered light pulse wave forms during $\text{d}I/\text{d}t$ test. Laser diode 150 mW was used in test circuit for LTT triggering. Capacitor charge voltage $V_C = 4000$ V.
It can be seen from figure 8 that developed LTT can commutate current pulses with \( \frac{di}{dt} = 5000 \, \text{A/}\mu \text{s} \). Tests with higher \( \frac{di}{dt} \) were not carried out due to limited test circuit capability.

Developed devices were tested in high voltage stack with 3 LTT in series connections (figure 9) for power capacitive storage device 5 kV, 50 kJ. Figure 10 shows equivalent circuit of storage device.

Power stack with 3 LTTs was tested in capacitive storage device. The stack sustained 1000 discharge cycles with peak pulse current 108-110 kA. Figure 11 shows current and voltage wave forms for LTT with blocking voltage 4.2 kV.

Temperature jump during current pulse affects the life time of semiconductor pulse switches. Calculation of structure maximum temperature can be used as theoretical confirmation for LTT robustness in pulse operation mode. Simulation model was used that takes into account semiconductor structure layout and dependence of turn-on condition spreading velocity on current density.

Figure 12 shows simulated temporal course of semiconductor structure temperature during current pulse 100 kA. The maximum temperature not exceeds 150°C that is much lower than critical temperature for semiconductor structure destruction (400-600 °C).

The main parameters of new developed LTT type TF193-2500 for pulsed power applications are presented in table 2.

<table>
<thead>
<tr>
<th>Item</th>
<th>Parameter name</th>
<th>Parameter value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Repetitive reverse voltage and repetitive peak forward off-state voltage, ( V_{RRM}, V_{FSRM} ), V</td>
<td>4200-5000</td>
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<tr>
<td>2</td>
<td>Peak pulse on-state current, ( i_{p} = 700 , \mu \text{s}, I_{p, \text{RM}}, \text{kA} )</td>
<td>110</td>
</tr>
<tr>
<td>3</td>
<td>Surge non-repetitive on-state current, ( I_{T, \text{RM}}, \text{kA} )</td>
<td>50</td>
</tr>
<tr>
<td>4</td>
<td>Critical rate of rise of on-state current, ( (\frac{di}{dt})_{\text{crit}}, \text{A/}\mu \text{s} )</td>
<td>5000</td>
</tr>
<tr>
<td>5</td>
<td>Critical rate of rise of off-state voltage, ( (\frac{dv}{dt})_{\text{crit}}, \text{V/}\mu \text{s} )</td>
<td>2000</td>
</tr>
<tr>
<td>6</td>
<td>Optic trigger power, ( P_{L}, \text{mW} )</td>
<td>40</td>
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<tr>
<td>7</td>
<td>Junction temperature, ( T_{j}, \degree \text{C} )</td>
<td>-40..+125</td>
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<td>8</td>
<td>Turn-off time (typical value), ( t_{q}, \mu \text{s} )</td>
<td>320</td>
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<td>9</td>
<td>Reverse recovery charge, ( Q_{\text{RR}}, \mu \text{As} )</td>
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</tr>
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<td>10</td>
<td>Weight, ( w, \text{kg} )</td>
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<tr>
<td>11</td>
<td>Clamping force, ( F, \text{kN} )</td>
<td>70..90</td>
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</table>

Table 2: Parameters of TF193-2500

Conclusion

This paper presents development and investigation results of high-voltage power LTTs. LTT is nowadays one of most important components for HVDC transmission equipment and for other applications in MW and GW power range, due to optical triggering, integrated protective functions and unique combination of load and commutation capabilities.

Tests show high reliability and effectiveness of LTTs. Works are being continued on LTT improvements – parameter, characteristics and functional capabilities optimization, additional self-protection elements implementation, losses reducing, operation voltage and commutated current increasing.

References


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